

How many capacitors per power pin?

In the past, TI (and many other semiconductor companies) recommended 1 capacitor(cap) per power pin. For DIP packages, this worked great, but other packages like BGAs were developed, this became harder and harder. With any pitch less than 1.0 mm this is nearly impossible, so now TI is trying to take a more realistic approach.

What is a pin inductance?

This is a useful concept for analyzing package AC noise and is widely used today. For example, a pin inductance is a partial-self inductance. Another useful term is the "open-loop" inductance which is the inductance of a loop with gaps at two ends.

How do you calculate the inductance of a decoupling capacitor?

When a chip and decoupling capacitor are both mounted on the top side of the package substrate, the inductance of the loop can be expressed as the sum of the inductances of the two half-loops above the top plane and the inductance of the loop between the planes.

How to reduce the inductance of a chip?

Vias should be placed close to each other to reduce the inductance of the path. In general, the inductance of structures on the chip is lower than the inductance of structures in the package and package inductances tend to be lower than inductances on the board.

Should high-frequency capacitance values be small to reduce stray inductance?

High-frequency capacitance values should be small to reduce the associated stray inductance. The placement of decoupling capacitors affects the overall effective inductance; therefore, a fairly complex package model that allows analysis of the effects of capacitor placement is usually necessary for power-distribution design.

Why do I need a lower inductance cap?

It plays a role only. Smaller, lower inductance caps go closer to the pins. They're most effective there; placing them farther away adds routing inductance and defeats their purpose. Take care when mixing values to avoid anti-resonance. This can cause cases where your decoupling is worse than the values by themselves.

The field of power electronics is concerned with the processing of electrical power using electronic devices [1-7]. The key element is the switching converter, illustrated in Fig. 1.1.

To provide this transient current, the path connecting the local decoupling capacitor to the power and ground pin of a device needs to have the lowest possible inductance. The local ...

The PDN in a PCB can be quite complex due to the use of multiple plane layers, power rails, vias leading to components, and decoupling capacitors used throughout. Each of these elements contributes some PDN ...

Block diagram of the test circuit and the parasitic inductance induced by the bonding wire. The test circuit includes a ring oscillator of 173-stage inverter chain and a decoupling capacitor.

A methodology for calculation of self- and mutual inductance of various electrical paths in a pin grid array (PGA) or a chip carrier package is described. For the highest speed and minimum ...

This is the 3rd low inductance capacitor technology developed by KYOCERA AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a ...

2 General Number and Value of Pin (bypass) Capacitors Required TI recommends placing one 0.1 mF cap (in the smallest possible package size, to reduce lead inductance) as close to the ...

Sigrity OptimizePI Capacitor to IC Device Loop Inductance
Analysis????????????IC?????,????????????,????,??????? ...

Both DC and AC Inductance can be provided for packages. To determine which inductance is appropriate for your application, please see the section "Frequency limitations of R-L-C ...

In PC board designs, paralleling of capacitors on a supply line is commonly used in an attempt to address interconnect inductance. A good discussion of this practice and the problems that result can be found in [1]. To illustrate the basic problem, consider an electronic circuit whose layout is shown in Figure 1. This is a top-view of a board with an 8-pin surface ...

The overall inductance of each connection is the sum of both lead and track inductances. Flat ceramic capacitors, matched to the common dual-in-line pinouts and intended for mounting directly beneath the IC package, minimize the pin-to-pin inductance and offer superior performance above about 50MHz.

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